

What is claimed is:

1. A nonvolatile semiconductor memory at least having a memory cell array structure that comprises:

5 active regions extending linearly in parallel with one another and containing impurity diffused source and drain regions;

element isolation regions extending linearly and isolating the active regions from one another;

10 gate electrodes orthogonally crossing the active regions and element isolation regions and each having a floating gate and a control gate laid one upon another;

first conductors extending linearly in parallel with the gate electrodes and each connecting the source regions to one another between adjacent ones of the gate electrodes; and

15 second conductors each having a discrete island shape and connected to one of the drain regions,

wherein the first and second conductors being formed from a single metal wiring layer.

20 2. The nonvolatile semiconductor memory of claim 1, wherein the memory cell array structure further comprises:

floating electrode isolation regions orthogonally crossing the gate electrodes and isolating the floating electrodes from one another.

25 3. The nonvolatile semiconductor memory of claim 1, wherein: the element isolation regions have trenches.

4. The nonvolatile semiconductor memory of claim 1, wherein: the memory cell array structure contains NOR memory cells.

30 5. The nonvolatile semiconductor memory of claim 1, wherein the memory cell array structure further comprises:

source contacts each connecting one of the source regions to a corresponding

one of the first conductors; and

drain contacts each connecting one of the drain regions to a corresponding one of the second conductors,

5 wherein the source contacts and drain contacts being symmetrical with each other about the gate electrodes,

the source regions and drain regions being symmetrical with each other about the gate electrodes.

6. The nonvolatile semiconductor memory of claim 5, wherein:
10 the source regions and drain regions substantially have an identical impurity concentration.

7. The nonvolatile semiconductor memory of claim 1, wherein a sheet resistance value of the single metal wiring layer is 1/1000 or below of a sheet
15 resistance value of the source regions.

8. The nonvolatile semiconductor memory of claim 1, wherein the first and second conductors are made of a copper.

20 9. A nonvolatile semiconductor memory at least having a memory cell array structure that comprises:

active regions extending linearly in parallel with one another and containing impurity diffused source and drain regions;

25 element isolation regions extending linearly and isolating the active regions from one another;

gate electrodes orthogonally crossing the active regions and element isolation regions and each having a floating gate and a control gate laid one upon another;

30 first conductors formed from a first metal wiring layer, the first conductors extending linearly in parallel with the gate electrodes and each connecting the source regions to one another between adjacent ones of the gate electrodes; and

second conductors formed from a second metal wiring layer that is above the first metal wiring layer, the second conductors orthogonally crossing the gate

electrodes and connected to the drain regions through contacts.

10. The nonvolatile semiconductor memory of claim 9, wherein the memory cell array structure further comprises:

5 floating electrode isolation regions orthogonally crossing the gate electrodes and isolating the floating electrodes from one another.

11. The nonvolatile semiconductor memory of claim 9, wherein:
the element isolation regions have trenches.

12. The nonvolatile semiconductor memory of claim 9, wherein:
the memory cell array structure contains NOR memory cells.

13. The nonvolatile semiconductor memory of claim 9, wherein the memory cell array structure further comprises:

15 source contacts each connecting one of the source regions to a corresponding one of the first conductors; and

drain contacts each connecting one of the drain regions to a corresponding one of the second conductors,

20 wherein the source regions and drain regions being symmetrical with each other about the gate electrodes.

14. The nonvolatile semiconductor memory of claim 13, wherein:
the source regions and drain regions substantially have an identical impurity
25 concentration.

15. The nonvolatile semiconductor memory of claim 13, wherein:
a bit line and the second conductors are being connected further than the first
conductors in a upper layer.

16. The nonvolatile semiconductor memory of claim 9, wherein a sheet
resistance value of the first conductors is 1/1000 or below of a sheet resistance value

of the source regions.

17. The nonvolatile semiconductor memory of claim 9, wherein:
the first conductors is made of material selected from a group consisting of
5 aluminum and aluminum-based alloys.

18. The nonvolatile semiconductor memory of claim 9, wherein the first and
second conductors are made of a copper.

10 19. A semiconductor device at least having a memory cell array that
comprises:
active regions extending linearly in parallel with one another at
predetermined intervals and each containing alternating source and drain regions;
gate electrodes orthogonally crossing the active regions between the source
15 and drain regions and each having a floating gate and a control gate laid one upon
another;
first conductors extending linearly in parallel with the gate electrodes and
connected to corresponding ones of the source regions through source contacts; and
second conductors connected to corresponding ones of the drain regions
20 through drain contacts.

20. The semiconductor device of claim 19, wherein:
the first and second conductors are formed from a single metal wiring layer;
and
25 the second conductors are discretely arranged above the drain regions,
respectively.

21. The semiconductor device of claim 19, wherein:
the second conductors are formed from a metal wiring layer that is above a
30 metal wiring layer from which the first conductors are formed, and orthogonally cross
the gate electrodes.

22. The semiconductor device of claim 19, wherein:
the memory cell array forms a flash memory.

23. The semiconductor device of claim 19, further comprising:
5 a logic device formed on the same chip on which the memory cell array is
formed.

24. The semiconductor device of claim 19, wherein the first and second
conductors are made of a copper.

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